IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Subhas Bothra, et al.	Grp./Art Unit : 1775
Appl. No	:	09/523,403	Examiner: S. Stein
Filed	:	March 10, 2000	
Title	:	Method of Using Films Having Optimized Optical Properties for Chemical Mechanical Polishing Endpoint Detection	
Docket No.	:	PHA 51101A (New) VLSI-3211.DIV (Previous)	

Assistant Commissioner for Patents
Washington DC 20231

RESPONSE and AMENDMENT

Sir:

This is in response to the Office Action of May 29, 2002.

IN THE CLAIMS

Please cancel Claims 14-18 without prejudice or disclaimer.

Please add new Claims 32-43 as follows.

32. (New) A structure, comprising:

a substrate;

a first patterned conductive line disposed on the substrate;

a first dielectric layer disposed superjacent the first patterned conductive line and the substrate, the first dielectric layer having a planarized surface;

a second patterned conductive line disposed on the planarized upper surface of the first dielectric layer;

a second dielectric layer disposed over the second patterned conductive line and that portion of the planarized upper surface of the first dielectric layer not

covered by the second patterned conductive line, the second dielectric layer having a surface including an uppermost planarized region substantially located above the second patterned conductive line, and further including non-planarized surface portions recessed downwardly from the plane of the uppermost planarized region;

an anti-reflective layer disposed on the non-planarized surface portions of the second dielectric layer; and

a third dielectric layer disposed superjacent the anti-reflective layer, the third dielectric layer having a planarized upper surface that is substantially coplanar with the planarized upper surface of the second dielectric layer.

33. (New) The structure of Claim 32, wherein the first patterned conductive line and the second patterned conductive line each comprise metal.

34. (New) The structure of Claim 32, wherein the anti-reflective layer comprises a material selected from the group consisting of amorphous silicon and silicon oxynitride.

35. (New) The structure of Claim 32, wherein the substrate comprises a semiconductor wafer.

36. (New) A structure, comprising:

at least one patterned conductive line disposed on a substrate;

a dielectric structure disposed over the at least one patterned conductive line, the dielectric structure comprising a first portion overlying the at least one patterned conductive line, the first portion being free from anti-reflective material, and a second portion overlying that portion of the substrate not covered by the at least one patterned conductive line, the second portion including a layer of anti-reflective material.

37. (New) The structure of Claim 36, wherein the dielectric structure has a planarized surface, and the layer of anti-reflective material is non-planar.

38. (New) The structure of Claim 37, wherein the anti-reflective material comprises a material selected from the group consisting of amorphous silicon and silicon oxynitride.

39. (New) The structure of Claim 38, wherein the substrate includes a semiconductor wafer.

40. (New) A structure, comprising:

a dielectric layer having a light-transmissive region disposed above, and substantially aligned with, an underlying patterned conductive line, and a non-light-transmissive region surrounding the light-transmissive region.

41. (New) The structure of Claim 40, wherein the non-light-transmissive region

includes a non-planar anti-reflective layer embedded therein.

42. (New) The structure of Claim 41, wherein the anti-reflective layer comprises a material selected from the group consisting of amorphous silicon and silicon oxynitride.

43. (New) The structure of Claim 42, wherein the dielectric layer is disposed over a semiconductor wafer.

REMARKS

This is in response to the Office Action of May 29, 2002. Claims 14-18 are pending in the application, and all the pending Claims 14-18, have been rejected.

Claims 14-18 have been cancelled, and new Claims 32-43 have been added.

No new matter has been added.

In view of the amendments above and remarks below, Applicant respectfully requests reconsideration and further examination.

About The Invention

The present invention relates generally to structures suitable for use in integrated circuits, and more particularly relates to structures that facilitate end point detection during chemical-mechanical polishing. Various embodiments of the present invention include a dielectric layer having a non-planar layer of anti-reflective material embedded therein, wherein there are openings, or gaps, in the embedded anti-reflective layer such that at least of portion of the light that is incident upon the region of the gaps, may be reflected back out through those

gaps.

Rejections under 35 USC 103(a)

Claims 14 and 17-18 have been rejected under 35 USC 103(a), as being obvious over Chung (US Patent 5,792,707). Claims 15-16 have been rejected under 35 USC 103(a), as being obvious over Chung and further in view of Hause (US Patent 6,013,574).

Claims 14-18 have been cancelled.

In view of these amendments, it is respectfully submitted that these rejections have been rendered moot.

New Claims 32-43

New Claims 32-43 have been added. These Claims are directed to structures that include a dielectric structure having a non-planar anti-reflective layer therein, where there are windows through the anti-reflective layer. Such structures are suitable for use within integrated circuits.

Support for these structures can generally be found throughout the specification; and can more particularly be found in the specification at page 21, line 21, through page 23, line 11, and in Fig. 6B.

The structures defined by new Claims 32-43 do not appear to be disclosed, in the cited references, nor does there appear to be a suggestion or motivation for making the Claimed structures.

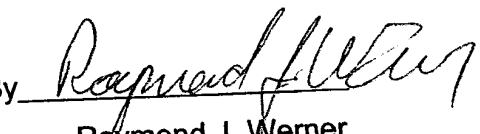
Conclusion

All of the rejections in the outstanding Office Action of May 29, 2002 have been responded to, and Applicants respectfully submit that the pending Claims 32-43 are now in condition for allowance.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "**Version with markings to show changes made**".

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

By 

Raymond J. Werner
Reg. No. 34,752

Dated: September 30, 2002
Portland, Oregon

Version with markings to show changes mad

In the Claims

32. (New) A structure, comprising:

a substrate;

a first patterned conductive line disposed on the substrate;

a first dielectric layer disposed superjacent the first patterned conductive line and the substrate, the first dielectric layer having a planarized surface;

a second patterned conductive line disposed on the planarized upper surface of the first dielectric layer;

a second dielectric layer disposed over the second patterned conductive line and that portion of the planarized upper surface of the first dielectric layer not covered by the second patterned conductive line, the second dielectric layer having a surface including an uppermost planarized region substantially located above the second patterned conductive line, and further including non-planarized surface portions recessed downwardly from the plane of the uppermost planarized region;

an anti-reflective layer disposed on the non-planarized surface portions of the second dielectric layer; and

a third dielectric layer disposed superjacent the anti-reflective layer, the third dielectric layer having a planarized upper surface that is substantially coplanar with the planarized upper surface of the second dielectric layer.

33. (New) The structure of Claim 32, wherein the first patterned conductive line and the second patterned conductive line each comprise metal.

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35. (New) The structure of Claim 32, wherein the substrate comprises a semiconductor wafer.

36. (New) A structure, comprising:

at least one patterned conductive line disposed on a substrate;

a dielectric structure disposed over the at least one patterned conductive line, the dielectric structure comprising a first portion overlying the at least one patterned conductive line, the first portion being free from anti-reflective material, and a second portion overlying that portion of the substrate not covered by the at least one patterned conductive line, the second portion including a layer of anti-reflective material.

37. (New) The structure of Claim 36, wherein the dielectric structure has a planarized surface, and the layer of anti-reflective material is non-planar.

38. (New) The structure of Claim 37, wherein the anti-reflective material

comprises a material selected from the group consisting of amorphous silicon and silicon oxynitride.

39. (New) The structure of Claim 38, wherein the substrate includes a semiconductor wafer.

40. (New) A structure, comprising:

a dielectric layer having a light-transmissive region disposed above, and substantially aligned with, an underlying patterned conductive line, and a non-light-transmissive region surrounding the light-transmissive region.

41. (New) The structure of Claim 40, wherein the non-light-transmissive region includes a non-planar anti-reflective layer embedded therein.

42. (New) The structure of Claim 41, wherein the anti-reflective layer comprises a material selected from the group consisting of amorphous silicon and silicon oxynitride.

43. (New) The structure of Claim 42, wherein the dielectric layer is disposed over a semiconductor wafer.